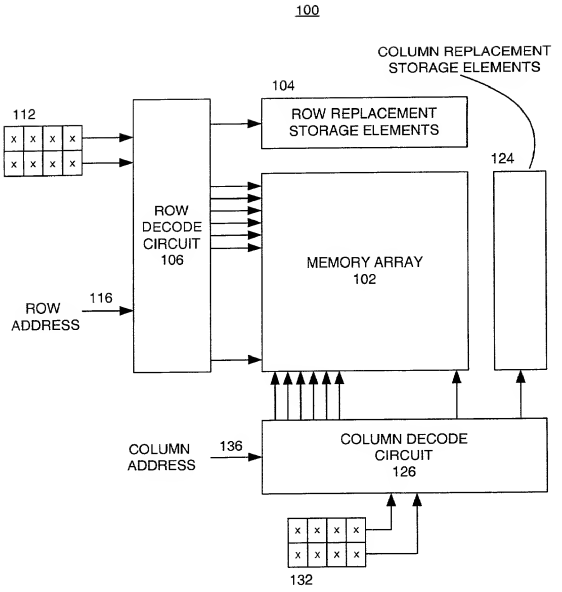
100
COLUMN REPLACEMENT STORAGE ELEMENTS
104
ROW REPLACEMENT STORAGE ELEMENTS
112
124
ROW DECODE CIRCUIT 106
MEMORY ARRAY 102
116
ROW ADDRESS
COLUMN ADDRESS
136
COLUMN DECODE CIRCUIT 126
132

FIG. 1

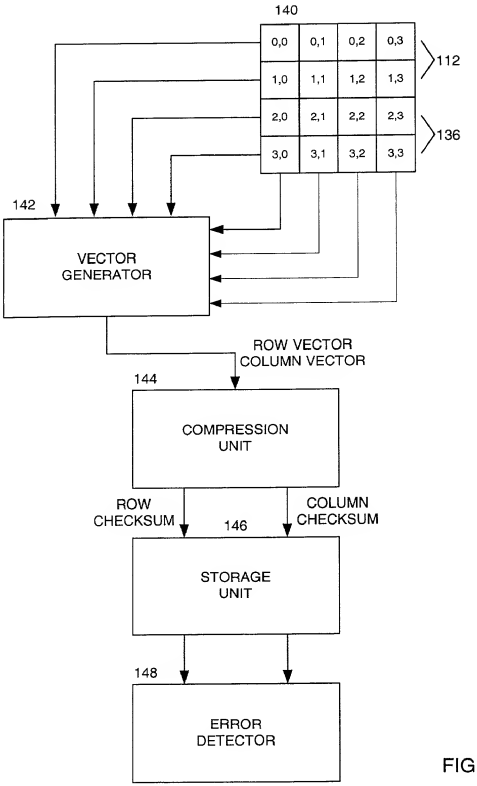
140
0,0
0,1
0,2
0,3
1,0
1,1
1,2
1,3
2,0
2,1
2,2
2,3
3,0
3,1
3,2
3,3
112
136
142
VECTOR GENERATOR
ROW VECTOR
COLUMN VECTOR
144
COMPRESSION UNIT
ROW CHECKSUM
COLUMN CHECKSUM
146
STORAGE UNIT
148
ERROR DETECTOR

FIG. 2

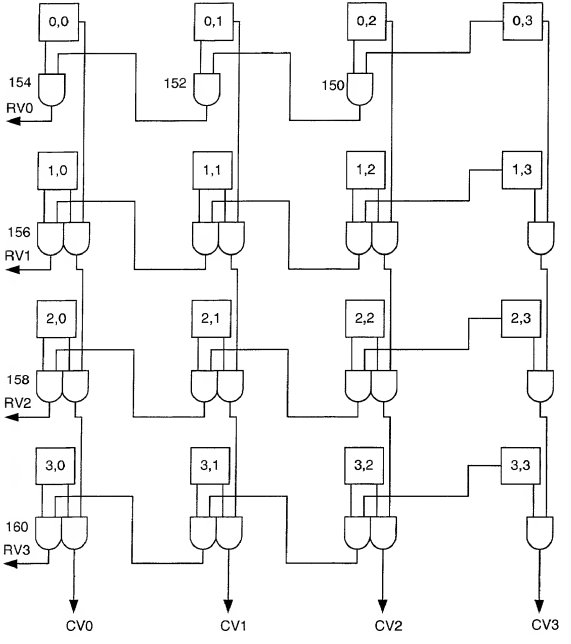
0,0
0,1
0,2
0,3
154
152
150
RV0
1,0
1,1
1,2
1,3
156
RV1
2,0
2,1
2,2
2,3
158
RV2
3,0
3,1
3,2
3,3
160
RV3
CV0
CV1
CV2
CV3

FIG. 3

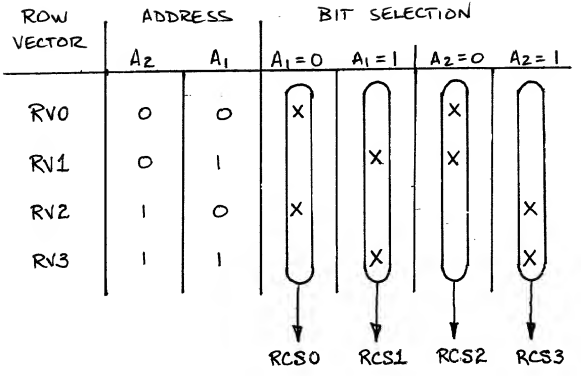
ROW VECTOR
ADDRESS
BIT SELECTION
A2
A1
A1 = 0
A1 = 1
A2 = 0
A2 = 1
RV0
RV1
RV2
RV3
0
0
0
1
1
0
1
1
X
X
X
X
X
X
X
X
RCS0
RCS1
RCS2
RCS3

FIG. 4

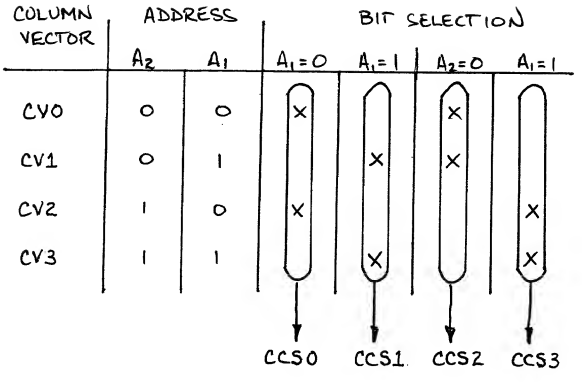
COLUMN VECTOR
ADDRESS
BIT SELECTION
A2
A1
A1=0
A1=1
A2=0
A1=1
CV0
CV1
CV2
CV3
0
0
0
1
1
0
1
1
X
X
X
X
X
X
X
X
CCS0
CCS1
CCS2
CCS3

FIG. 5

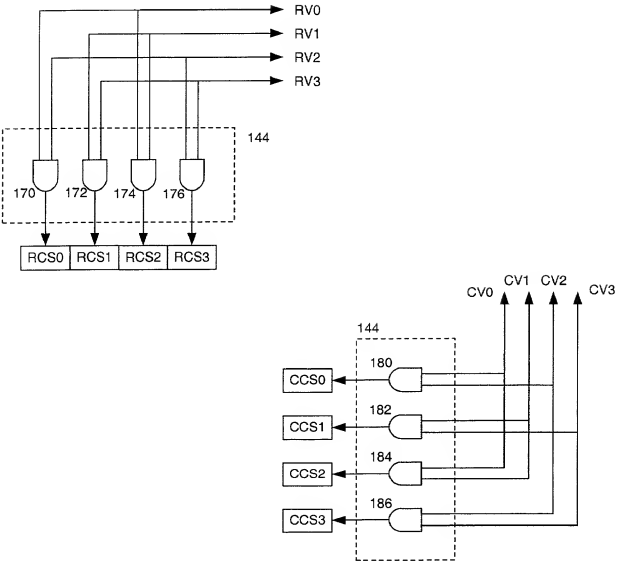
RV0
RV1
RV2
RV3
144
170
172
174
176
RCS0
RCS1
RCS2
RCS3
CV0
CV1
CV2
CV3
144
180
182
184
186
CCS0
CCS1
CCS2
CCS3

FIG. 6